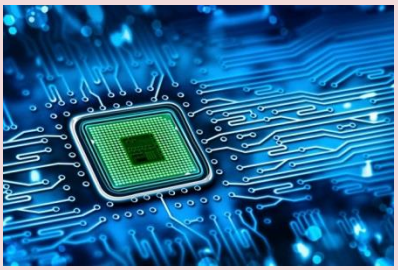
Workshop on "VLSI and Embedded System Design"

25th to 26th October, 2017



Keynote Speakers

Dr. Mijanur Rahaman
Associate Professor
Department of CSE
Uttara University (UU)

Mohammed Abdul Kader
Assistant Professor
Department of EEE
International Islamic University Chittagong, Bangladesh (IIUC)

Objectives :

- Advanced design and analysis of digital circuits with HDL.
- Provide in depth understanding of logic and system design.
- Enables participants to apply their knowledge for the design of VLSI systems with help of FPGA tools

Course Contents :

Session-I (Day-1 : 9AM to 12PM)
Introduction to FPGA, Verilog HDL, Schematic design in FPGA, Structural Verilog coding, RTL Verilog coding, Implementation of combinational circuits (Decoder, Multiplexer, Adder, and Code Converter circuit etc.) in FPGA by RTL Verilog coding.

Session-II (Day-1 : 2PM to 5PM)
Implementation of sequential circuits (Flip-Flops, Up-Counter, Down-Counter, Up/down counter, different types of Shift registers, RAM etc.) in FPGA by RTL Verilog coding.

Session-III (Day-2 : 9AM to 12PM)
Design of a display driver for multiple 7-segment display.

Session-IV (Day-2 : 2PM to 4PM)
VLSI- A big leap toward non-von Neumann Computation.

Session-V (Day-2 : 4PM to 5PM)
Certificate giving & Closing Ceremony

Venue, Date & Time :

Venue: Simulation Lab, Dept. of EEE, Uttara University
House-4 , Road-15, Sector-6, Uttara, Dhaka-1230.
Date: 25th to 26th October, 2017
Time: 9AM to 5 PM (both days)

Registration :

Registration Fees : 1500.BDT
Available Seats : Only **16** Persons
Registration Deadline : 3:00PM, 24th October, 2017.

Contact Persons :

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Organized by :
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